IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): A.Q. Khan et al.
Case: 4-14-28
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Group: 2619
Examiner: Brian T. O'Connor

Title: Processor with Scheduler Architecture Supporting Multiple Distinct Scheduling Algorithms

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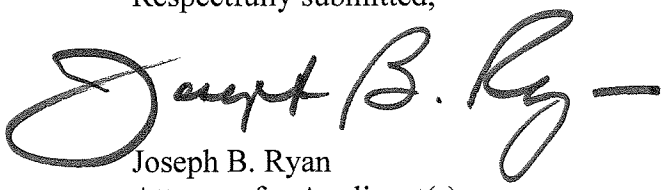
RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notification of Non-Compliant Appeal Brief dated June 19, 2008, with reference to the Appeal Brief filed June 9, 2008, Applicants submit herewith a revised Summary of Claimed Subject Matter in accordance with MPEP 1205.03(B).

Respectfully submitted,



Date: June 30, 2008

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SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor comprising scheduling circuitry operative to schedule data blocks for transmission from a plurality of transmission elements. The scheduling circuitry is configurable for utilization of at least a first table and a second table in scheduling the data blocks for transmission. The processor further comprises memory circuitry associated with the scheduling circuitry and configurable to store at least a portion of at least one of the first and second tables.

The first table is configurable to include at least first and second lists of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a first scheduling algorithm. The scheduler is operative to maintain a first table pointer identifying at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table.

The second table is configurable to include a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a second scheduling algorithm different than the first scheduling algorithm. Association of a given one of the transmission elements with a particular one of the entries establishes a scheduling rate for that transmission element. The scheduler maintains a second table pointer identifying a current one of the second table entries as being eligible for transmission.

In an illustrative embodiment shown in FIG. 3, a processor (e.g., processor 102 in FIG. 2) comprises scheduling circuitry (e.g., scheduler 300 in FIG. 3) operative to schedule data blocks for transmission from a plurality of transmission elements (e.g., transmit queues 302 in FIG. 3); see, e.g., the specification at page 7, lines 11-19. The scheduling circuitry is configurable for utilization of at least a first table (e.g., FIFO lists 310 in FIG. 3) and a second table (e.g., dynamic calendar table 312 in FIG. 3) in scheduling the data blocks for transmission; see, e.g., the specification at page 7, lines 19-22. The processor further comprises memory circuitry (e.g., internal memory 104 in FIG. 1) associated with the scheduling circuitry and configurable to store at least a portion of at least one of the first and second tables; see, e.g., the specification at page 8, lines 13-17.

As described in the specification at page 9, line 26, to page 10, line 15, with respect to an illustrative embodiment shown in FIG. 4, the first table is configurable to include at least first and second lists (e.g., FIFO List 1, FIFO List 2, etc. in FIG. 4) of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a first scheduling algorithm. The scheduler is operative to maintain a first table pointer (e.g., ActiveList Pointer in FIG. 4) identifying at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table.

As described in the specification at page 11, line 14-24, with respect to an illustrative embodiment shown in FIG. 5, the second table is configurable to include a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a second scheduling algorithm different than the first scheduling algorithm. Association of a given one of the transmission elements with a particular one of the entries establishes a scheduling rate for that transmission element. The scheduler maintains a second table pointer (e.g., CurrentPointer in FIG. 5) identifying a current one of the second table entries as being eligible for transmission.

Independent claim 19 is directed to a method for use in a processor. The method comprises storing at least a portion of at least one of a first table and a second table; and scheduling data blocks for transmission from a plurality of transmission elements, utilizing the first and second tables.

The first table is configurable to include at least first and second lists of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a first scheduling algorithm. A first table pointer identifies at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table.

The second table is configurable to include a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a second scheduling algorithm different than the first scheduling algorithm. Association of a given one of the transmission elements with a particular one of the entries establishes a scheduling rate

for that transmission element. A second table pointer identifies a current one of the second table entries as being eligible for transmission.

As described with respect to an illustrative embodiment in FIG. 3, a method for use in a processor (e.g., processor 102 in FIG. 2) includes storing (e.g., within internal memory 104 in FIG. 1) at least a portion of at least one of a first table (e.g., FIFO lists 310 in FIG. 3) and a second table (e.g., dynamic calendar table 312 in FIG. 3); see, e.g., the specification at page 8, lines 13-17. The method also includes scheduling data blocks for transmission from a plurality of transmission elements (e.g., transmit queues 302 in FIG. 3) utilizing the first and second tables; see, e.g., the specification at page 7, lines 11-22.

As described in the specification at page 9, line 26, to page 10, line 15, with respect to an illustrative embodiment shown in FIG. 4, the first table is configurable to include at least first and second lists (e.g., FIFO List 1, FIFO List 2, etc. in FIG. 4) of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a first scheduling algorithm. A first table pointer (e.g., ActiveList Pointer in FIG. 4) identifies at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table.

As described in the specification at page 11, line 14-24, with respect to an illustrative embodiment shown in FIG. 5, the second table is configurable to include a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a second scheduling algorithm different than the first scheduling algorithm. Association of a given one of the transmission elements with a particular one of the entries establishes a scheduling rate for that transmission element. A second table pointer (e.g., CurrentPointer in FIG. 5) identifies a current one of the second table entries as being eligible for transmission.

Independent claim 20 is directed to an article of manufacture comprising a computer-readable medium for use in conjunction with a processor. The medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements. The one or more programs when executed implement the step of

scheduling data blocks for transmission from a plurality of transmission elements, utilizing first and second tables.

The first table is configurable to include at least first and second lists of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a first scheduling algorithm. A first table pointer identifies at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table.

The second table is configurable to include a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a second scheduling algorithm different than the first scheduling algorithm. Association of a given one of the transmission elements with a particular one of the entries establishes a scheduling rate for that transmission element. A second table pointer identifies a current one of the second table entries as being eligible for transmission.

As described in the specification at, for example, page 7, lines 3-10, with respect to an illustrative embodiment shown in FIG. 2, an article of manufacture may comprise a computer-readable medium for use in conjunction with a processor (e.g., processor 102 in FIG. 2). As described in the specification at, for example, page 7, lines 11-22, with respect to an illustrative embodiment shown in FIG. 3, the medium stores one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements (e.g., transmit queues 302 in FIG. 3). The one or more programs, when executed, implement the step of scheduling data blocks for transmission from a plurality of transmission elements, utilizing first (e.g., FIFO lists 310 in FIG. 3) and second (e.g., dynamic calendar table 312 in FIG. 3) tables.

As described in the specification at page 9, line 26, to page 10, line 15, with respect to an illustrative embodiment shown in FIG. 4, the first table is configurable to include at least first and second lists (e.g., FIFO List 1, FIFO List 2, etc. in FIG. 4) of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a first scheduling algorithm. A first table pointer (e.g., ActiveList Pointer in FIG. 4) identifies at least one of the first and second lists of the first table as having priority over the other of the first and second lists of the first table.

As described in the specification at page 11, line 14-24, with respect to an illustrative embodiment shown in FIG. 5, the second table is configurable to include a plurality of entries corresponding to transmission elements for which data blocks are to be scheduled in accordance with at least a second scheduling algorithm different than the first scheduling algorithm. Association of a given one of the transmission elements with a particular one of the entries establishes a scheduling rate for that transmission element. A second table pointer (e.g., CurrentPointer in FIG. 5) identifies a current one of the second table entries as being eligible for transmission.

Illustrative embodiments of the claimed invention provide a number of significant advantages over conventional arrangements. As discussed in the specification at, for example, page 2, lines 1-8, and page 6, lines 4-14, an illustrative embodiment of the present invention provides an efficient and flexible scheduler architecture capable of supporting multiple scheduling algorithms. The architecture is particularly advantageous in the network processor context in that it provides sufficient flexibility to allow the implementation of new algorithms as they are defined without requiring redesign of the hardware or other elements of the network processor. Rather, a wide variety of scheduling algorithms may be implemented within a single network processor, under software control, thereby avoiding the need for separate hardware architectures to support each of the desired scheduling algorithms.